501.37436CV2

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicants: NISHIHARA et al.

Serial No.: Rule 53(b) of 09/380,735

Filed: November 26, 2003

For: METHOD OF FABRICATING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

Art Unit: Unassigned (2811 previously in parent application)

Examiner: Unassigned (D. Kang previously in parent application)

**INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 AND §1.98**

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

November 26, 2003

Sir:

Pursuant to Applicants' duty of disclosure, enclosed please find a List, on a form substantially equivalent to Form PTO-1449, of documents cited in connection with a prior application of the above-identified application, Application No. 09/380,735, given a filing date in view of 35 USC §371 of February 4, 2000. The enclosed List also includes thereon the enclosed article by Takao, et al., from the 1997 Symposium on VLSI Technology Digest of Technical Papers.

Apart from the enclosed article by Takao, et al., all other documents on the enclosed List were either cited by the Examiner during prosecution of Application No. 09/380,735 or were cited by Applicants, on a proper form substantially equivalent to Form PTO-1449, in Application No. 09/380,735. Since Application

No. 09/380,735 is being relied upon in the above-identified application under 35 USC §120, copies of the listed documents, except for the aforementioned Takao, et al., article, are not enclosed.

This Information Disclosure Statement is being submitted concurrently with the filing of the above-identified application. Accordingly, requirements of 37 CFR §1.97(b) are satisfied.

In view of the foregoing, it is respectfully submitted that all applicable requirements of 37 CFR §1.97 and §1.98 have been satisfied, in connection with each of the documents on the enclosed List. Accordingly, consideration of the listed documents, upon examination of the above-identified application, is respectfully requested.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees and excess claim fees, to Deposit Account No. 01-2135 (referencing case No. 501.37436CV2) and please credit any excess fees to such deposit account.

Respectfully submitted,

Alan E. Schiavelli
Registration No. 32,087
ANTONELLI, TERRY, STOUT & KRAUS, LLP

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(703) 312-6600

| Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | ATTY. DKT. NO. | APPLICATION NO. |
|---|---|---|
| | 501.37436VC2 | TBD |
| **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** | **APPLICANT** Nishihara, et al. | |
| **(Use several sheets if necessary)** | **FILING DATE** November 26, 2003 | **EXPECTED GROUP** 2811 |

**U.S. PATENT DOCUMENTS**

| Examiner Initial | | Document Number | Date | Name | Class | Subclass | Filing Date |
|---|---|---|---|---|---|---|---|
| | AA | 5,691,225 | 11/25/1997 | Abiko | | | |
| | AB | 5,652,176 | 7/29/1997 | Maniar, et al. | | | |
| | AC | 5,736,461 | 4/7/1998 | Berti, et al. | | | |
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**FOREIGN PATENT DOCUMENTS**

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|---|---|---|---|---|---|---|---|---|
| | AE | | | | | | | |
| | AF | | | | | | | |
| | AG | | | | | | | |

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

| | | |
|---|---|---|
| | AH | Chinese Office Action dated December 27, 2002, for corresponding Application No. 97182025.2 with English Translation |
| | AI | Patent Abstracts of Japan, for Publication No. 07003486A, published January 6, 1995 |

| Examiner | Date Considered |
|---|---|
| | |

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard St.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC

| FORM PTO-1449 U.S. Department of Commerce (Rev. 4/92) Patent and Trademark Office | ATTY. DOCKET NO. | APPLICATION NO. |
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|---|---|---|---|---|---|---|---|
| | | 5,998,284 | 12/07/1999 | Azuma | | | |
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| | | | | | | | YES | NO |
| | | 6-192874 | 07/12/1994 | Japan | | | X | |
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| | | W.T. Lynch, et al., Self-Aligned Contact Schemes For Source-Drains In Submicron Devices, 1987, pps. 354-357, IEEE |
| | | Shyam P. Muraka, Self-aligned silicides or metals for very large scale integrated circuit applications, Nov/Dec 1986, pps. 1325-1331, J. Vac. Sci. Technol. B 4 (6) |
| | | Eiji Nagasawa, et al., Mo- and Ti-Silicided Low-Resistance Shallow Junctions Formed Using th Ion Implantation Through Metal Technique, March 1987, IEEE Transactions On Electron Devices, Vol. Ed-34, No. 3 |

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**EXAMINER: Initial if citation is considered, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.**

| FORM PTO-1449 U.S. Department of Commerce (Rev. 4/92) Patent and Trademark Office | ATTY. DOCKET NO. | APPLICATION NO. |
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| | | J.M. Poate, Silicide Formation, Thin Films - Interdiffusion and Reactions, pps. 359-405 |
| | | Thomas E. Tang, et al., Titanium Nitride Local Interconnect Technology for VLSI, March 1987, pps. 682-688, Electron Devices, Vol. Ed-34, No. 3 |
| | | R.D.J. Verhaar, et al., Self-aligned $CoSi_2$ in a Submicron CMOS Process, pps. 229-232 |
| | | Takao, et al., "A 4-um$^2$ Full-CMOS SRAM Cell Technology for 0.2-um High-Performance Logic LSIs", 1997 Symposium on VLSI Technology Digest of Technical Papers, pages 11 and 12 |
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|---|---|
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(Form PTO-1449 [6-4])

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| | | Chih-Yuan Lu, et al., A Folded Extended Window MOSFET for ULSI Applications, August 1988, pps. 388-390, IEEE Electron Device Letters, Vol. 9, No. 8 |

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